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HONEYWELL
INFORMATION
SYSTEMS INC.

C66-91

TITLE:

No. 43A177879

ENGINEERING PRODUCT SPECIFICATION, PART 1

MPC - PSI LINK ADAPTER

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REVISION RECORD

REVISION LETTER	DATE	PAGES AFFECTED	APPROVALS	AUTHORITY
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A ISSUED

MAY 14 1971

PSI 2-15.1
16-42F

HONEYWELL PROPRIETARY

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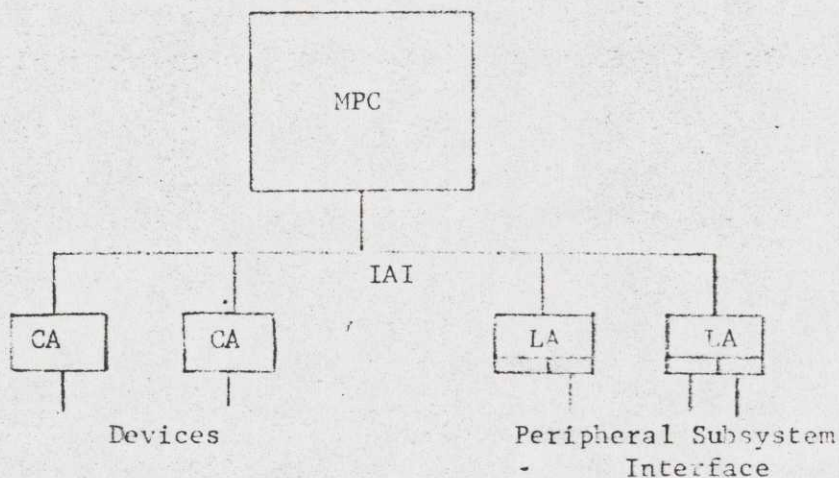
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2.0

GENERAL

The Link Adapter is a hardware communication module with the necessary logical and storage capabilities to connect the MPC to the Peripheral Subsystem Interface. The Link Adapter is controlled by the MPC firmware through the Internal Adapter Interface (IAI). Two LA's per MPC are possible.



CA = Controller Adapter

2.1

Main Characteristics

The Link Adapter will be packaged in the same cabinet as the MPC. This allows a synchronous dialog on the IAI and the synchronization of the signals exchanged on the Peripheral Subsystem Interface by the clocks generated within the MPC.

The main functions implemented in the Link adaptor are:

- Switching of two Peripheral Subsystem Interface channels.
- Electrical separation between the Peripheral Subsystem Interface and the Internal Adapter Interface.
- Signal translation and synchronization between the two interfaces

1.0

INTRODUCTION

The purpose of this document is to specify the characteristics and operation of a Peripheral Subsystem Interface Link Adapter (LA) and the basic MPC firmware controls necessary to bring about appropriate interaction between the LA and the Central Processor Complex (CPU or IOC) through the Peripheral Subsystem Interface (PSI). This LA adapts a "one byte" PSI to a Microprogrammed Peripheral Controller

2.1 (continued)

- Data buffering
- Service Code buffering
- Buffering of some control lines
- Error checking.

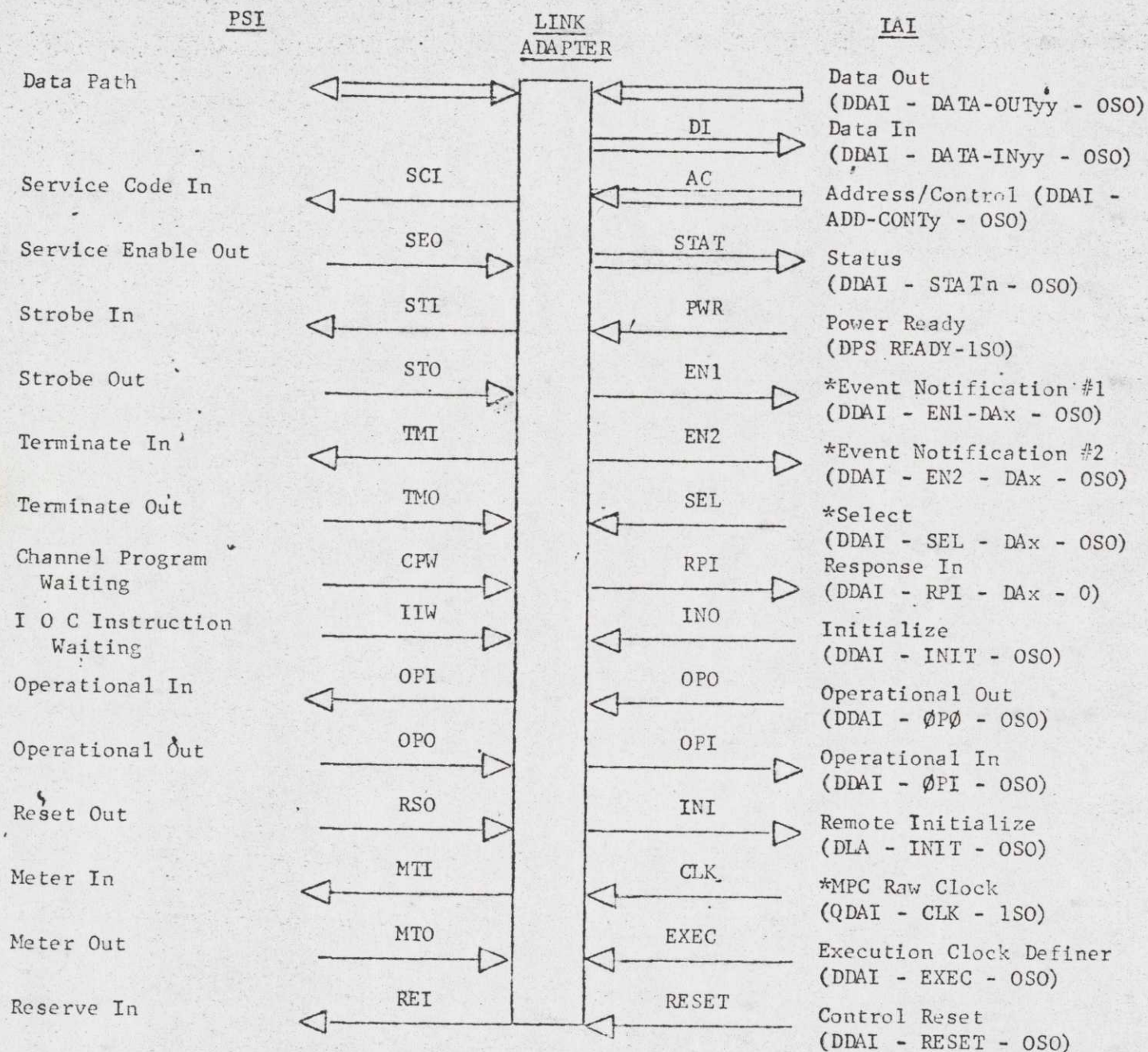
2.2 Applicable Documents

The following documents support this specification:

- Peripheral Subsystem Interface Specification --- 43A177874
- Basic Microprogrammed Peripheral Controller Specification --- 43A177875
- MPC Internal Adapter Interface Specification --- 43A177876
- MPC Microprogram Reference Manual
- CE-655 General Design Requirements EPS-1 --- 43A177851
- Common MPC Maintainability Specification --- 43A237500

3.0 HARDWARE INTERFACE REQUIREMENTS

The LA operates with the Central Processor Complex through the Peripheral Subsystem Interface in conformance with the Engineering Product Specification #43A177874. The LA operates with the MPC through the backpanel Internal Adapter Interface in conformance with the EPS-1, #43A177876.



* Star lines on the IAI

Note: - yy; y & n designate Specific Line: yy = 00-15, P0, P1
y = 0-7, P n = 0-3, P
- x designates Adapter Port, and can be only 2 or 3 for LA's.

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4.0

FUNCTIONAL DESCRIPTION

The Link Adapter has two interfaces, one with the MPC through the backpanel IAI, the other with the Central Processor Complex (CPC) via the PSI.

The LA allows data transfer and service code transfer between the MPC and a CPC having the one byte data path PSI facility. Data transfer between the LA and the MPC is performed on the IAI on a two byte basis. The Link Adapter must be capable of operating at speeds consistent with the MPC and the Central Processor Complex.

The LA is transparent for all information transferred between the MPC and the external system, but parity errors are to be detected by the LA. Service codes to the external system are generated by the MPC microprogram.

Service codes from the external system are transferred in the form of data and interpreted by the MPC microprogram.

The LA contains storage registers and some hard wired control logic, but the major control is achieved by the Control Store microprograms of the MPC.

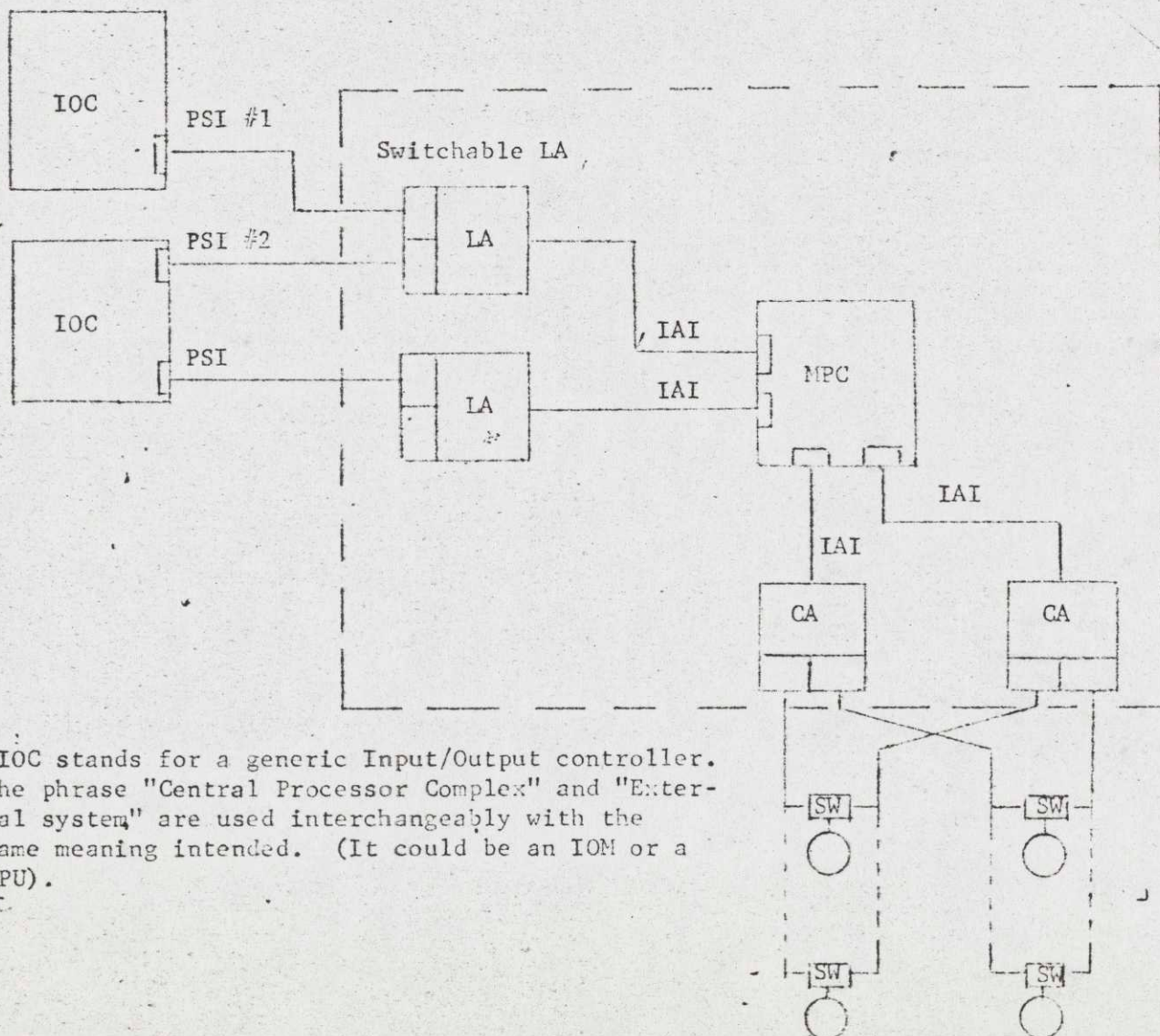
4.1

Two PSI Channel Switch Features

The Two-PSI channel switch is a standard hardware feature which provides the ability for the LA to be shared by two PSI physical channels. The two channels can be attached to the same IOC or to different IOC's. Channel switching is controlled by the MPC firmware. The LA has the capability to transfer data on a message basis over both PSI physical channels but not simultaneously. The LA receives the control lines "Channel Program Waiting" and "IOC Instruction Waiting" from both PSI channels and generates an Event Notification #2 to the MPC if any one of them is activated. These lines are readable under microprogram control.

The two PSI physical channels connected to the LA will be referenced as PSI #1 and PSI #2.

The following figure illustrates a high speed disc configuration which may be used with the Two-PSI channel switch feature.



*IOC stands for a generic Input/Output controller. The phrase "Central Processor Complex" and "External system" are used interchangeably with the same meaning intended. (It could be an IOM or a CPU).

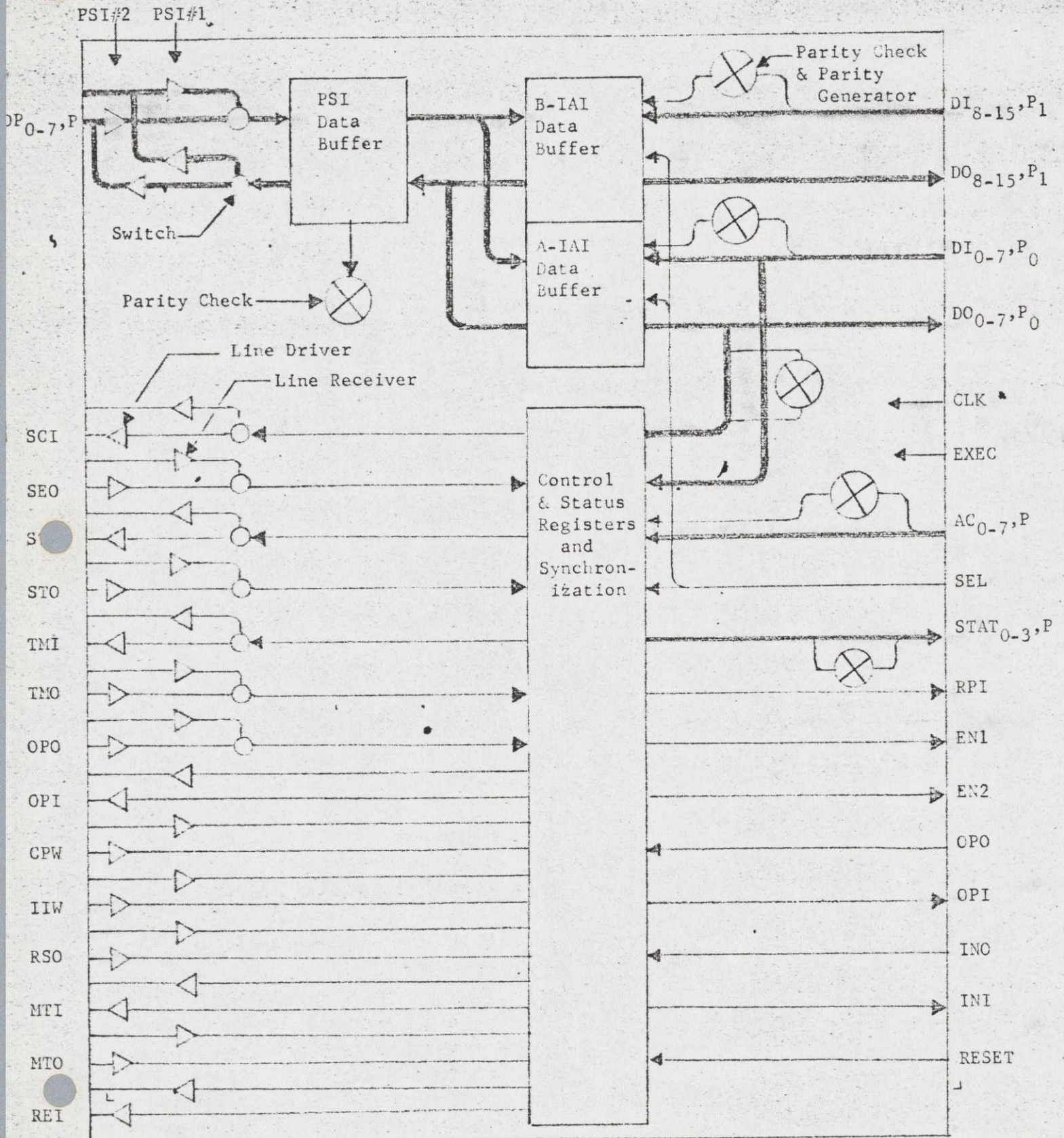
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LINK ADAPTER BLOCK DIAGRAM



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4.3 Logical Description

This specification is not intended to define a particular hardware implementation of the Link Adapter. The LA block diagram and the following descriptions are subject to modification as a result of engineering developments.

4.3.1 IAI Buffer Register

The IAI Buffer registers can be functionally used as a two byte buffer or split into two single byte buffers A and B.

Each single byte buffer consists of eight information bits and one odd-parity bit.

During a Write sequence, the IAI buffer receives data from the PSI Buffer register and can be read out on the IAI Data In bus by the MPC.

During a Read sequence, the IAI buffer is loaded with the content of the IAI Data Out bus under the control of the MPC. Then, the IAI Buffer contents are transferred, one byte at a time, to the PSI Buffer register.

The status of each single byte buffer is indicated by a flag which is a part of the control and status registers.

An Event Notification #1 is generated to the MPC depending upon the status of the buffer's flags.

4.3.2 PSI Buffer Register

This buffer consists of eight information bits and one odd parity bit; it permits data transfer on the PSI to take place concurrently with data transfer on the IAI.

During a Write sequence, the PSI buffer receives data from the PSI Data Path bus and can be read out to the IAI Buffer register.

During a Read sequence, the PSI buffer receives data from the IAI Buffer register and can be read out on the PSI Data Path bus.

The status of the PSI buffer is indicated by a flag which is a part of the control and status registers.

The PSI signal "Strobe In" is generated to the external system depending upon the status of the PSI Buffer flag.

Control and Status Registers

The control and status registers monitor and control the different dialog sequences in the Link Adapter. They are arranged as eight bit registers which can be set or reset by the MPC firmware through the Internal Adapter Interface.

The content of each register can be reflected on the IAI Data In bus with a TEST microcommand in order to be testable by the MPC firmware.

The registers defined in this paragraph are those registers which are directly visible by the MPC firmware. Other registers which are a function of the hardware implementation may be defined during the design phase.

3.1 LA Mode Register

This register provides the capability to set up the data transfer mode in the LA and to position the two-PSI switch.

This register can be read and loaded under microprogram control.

Bits will be provided in this register for the following functions:

Switch Selection

This bit indicates which of the two PSI channels is selected.

Read-Write

This bit indicates the direction of the data transfer.

Forward-Backward

This bit indicates whether the data is handled in a Forward or Backward mode.

Allow Parity Error

When this bit is set:

In a Write sequence, the data parity bit from the external system is transmitted to the MPC as received whether or not a parity error is being detected by the LA.

In a Read sequence, the data parity bit from the MPC is transmitted to the external system as received whether or not a parity error is being detected by the LA.

In either case, detected errors will be memorized in the Error Register.

4.3.3.2 EN.2 Register

This register provides storage for any cause of an EN.2.

The register can be read under microprogram control. Different causes of an EN.2 indicated by this register are:

- Channel Program Waiting on PSI #1
- Channel Program Waiting on PSI #2
- IOC Command Waiting on PSI #1
- IOC Command Waiting on PSI #2
- Operational Out Drop on PSI #1 *
- Operational Out Drop on PSI #2 *
- End of a Service Code Sequence.
- End of a data transfer sequence generated either by the MPC or by the external system.

The last four bits can be reset under microprogram control.

* Note: Any drop of the PSI line operational Out is trapped by the LA and any operation currently in process for that physical channel shall be reset by the MPC microprogram.

4.3.3.3 PSI Indicator Register

This register is split up into two four-bit registers. One is dedicated to the PSI #1, the other to the PSI #2.

Both registers are used to control or memorize the following lines of the Peripheral Subsystem Interface.

- Operational In *
- Reserve In
- Meter In
- Meter Out (Testable Only)

The two four-bit registers can be loaded independently and read simultaneously under microprogram control.

*Note: The PSI "Operational In" line reflects:

- basic MPC operational (IAI "Operational Out" line)
- LA operational ("Operation In" flip-flop of the PSI indicator register).

4.3.3.4 Error Register

This register provides storage for the indication of any error detected within the LA.

The register can be read and reset under microprogram control.

Different Errors indicated by this register are:

- Parity error on the IAI Address Control Bus
- Parity error within the PSI buffer (Data transfer In or Out)
- Parity error on the upper lines of the IAI Data Out bus, (DI 0-7).
- Parity error on the lower lines of the IAI Data Out bus, (DI 8-15).

4.3.4 LA States

The Link Adapter can be either in the "busy" state or in the "idle" state.

The Link Adapter enters the "busy" state when an I/O transaction is initiated by the MPC on the Peripheral Subsystem Interface and stays in this state until the completion of this transaction on both the PSI and the IAI interfaces.

The LA enters the "busy" state when the MPC microprogram initiates a service code sequence. It may stay in this state when the Service code sequence is completed if the service code initiates a data transfer sequence. The LA comes back to the "idle" state:

- At the end of a service code sequence which does not involve a following data transfer.
- At the end of a service code sequence if the PSI line "IOC Instruction Waiting" is up.
- At the end of a data transfer terminated either by the external system or the MPC, when the last byte has been transferred to the external system in the "read" mode or to the MPC in the "write" mode.
- If the PSI "Operational Out" line of the selected PSI drops.

The MPC is informed of the completion of an I/O transaction by an EN #2.

The LA sends such an EN #2 when going from the "busy" to the "idle" state and at the end of any service code sequence.

The cause of this EN #2 is testable by the MPC microprogram:

- terminate from the external system or from the MPC
- end of a service code sequence

In the "idle" state the lines of the IAI Data-In bus to the MPC reflect all zeros with the correct parity.

Note: The Link Adapter can be set "Non-operational" independantly for each PSI channel when it is unable to communicate through a physical channel.

When the LA is set "Non-operational" for one PSI channel, the corresponding "Operational In" line is dropped and all PSI/Out lines of that physical channel but "Reset Out" are ignored by the LA.

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4.3.5 LA Initialization

The PSI line "Reset Out" is directly transmitted by the LA to the MPC through the IAI line "Remote Initialize".

Whenever a remote or a local initialization of the MPC occurs the IAI signal "Initialize" sets the LA in a known state:

- Non-operational for both PSI channels
- Idle state
- Write-Forward mode
- PSI #1 Selected

4.4

LINK ADAPTER/MPC FIRMWARE INTERFACE

The Link Adapter is addressed and controlled by an MPC - DAI microinstruction.

The Argument 1 field of the microinstruction must define that the microinstruction execution is to wait for the IAI signal "Response In" from the LA.

If the "Wait for RPI" option is not used during data transfer operation, data may be lost without indication to the MPC.

The Argument 3 field of the microinstruction supplies the 8-bit LA microcommand to be sent over the IAI Address/Control lines during the microinstruction execution.

The LA port address is defined by the content of the LA field of the MPC-DA control register in relation with the content of the MPC-DA number register if the IAI microinstruction addresses a generic LA port.

The LA port address is defined by the content of the MPC-DA number register if the IAI microinstruction addresses a specific LA port. The LA port address can only be 2 or 3.

Each microcommand carried out in the Link Adapter will result in status being reflected on the status lines of the IAI. Status is sent along with "Response In" to the MPC. If a parity error is detected on the IAI Address/Control lines by the LA, the microcommand is ignored; status reflecting the error is sent along with "Response In" to the MPC. A parity error detected by the LA on the IAI Data lines does not prevent a microcommand from being executed; status reflecting the error is sent back to the MPC.

There are five basic microcommands defined on AC₀₋₂:

- Set LA
- Data Transfer
- Service Code Transfer
- Test LA
- Clear LA

AC₃₋₇ define submicrocommands used in conjunction with the first four basic microcommands.

Address/Control

0	1	2	3					7
X	X	X	X	X	X	X	X	X

Submicrocommands

1	0	0	Set LA
1	0	1	Data Transfer
1	1	0	Service Code Transfer
1	1	1	Test LA
0	1	1	Clear LA

4.4.1 Set LA Microcommand

This microcommand defined by $AC_{0-2} = 100$ on the Address/Control lines of the IAI is used:

- to initialize the mode of operation of the LA and to position the two-PSI switch.
- to set or reset the flip-flops controlling the PSI lines
- to reset a flip-flop which memorizes an event taken into account by the MPC.
- for the purpose of diagnosis.

The flip-flops of the Link Adapter are arranged as 8-bit registers, referenced in binary from 000 to 111. The Set LA microcommand provides the capability to set or reset the flip-flops of the LA register addressed by AC_{5-7} according to the binary information transmitted on the 8 lower lines of the IAI Data Out bus (DO_{8-15}).

Address/Control	0	2	3	4	5	7
	1	0	0	X	X	X

Register #

AC_3 may be used in conjunction with a Set LA microcommand to set up the LA in the "busy" state.

AC_4 may be used in conjunction with a Set LA microcommand to indicate that only the four lower bits (4-7) or the four upper bits (0-3) of the addressed register have to be set or reset.

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4.4.1 (cont'd.)

The following Table shows the contents of the various LA registers which can be handled under microprogram control, either for a normal use or for the purpose of diagnosis. The letters L, R, C, associated with the register address are used as follows:

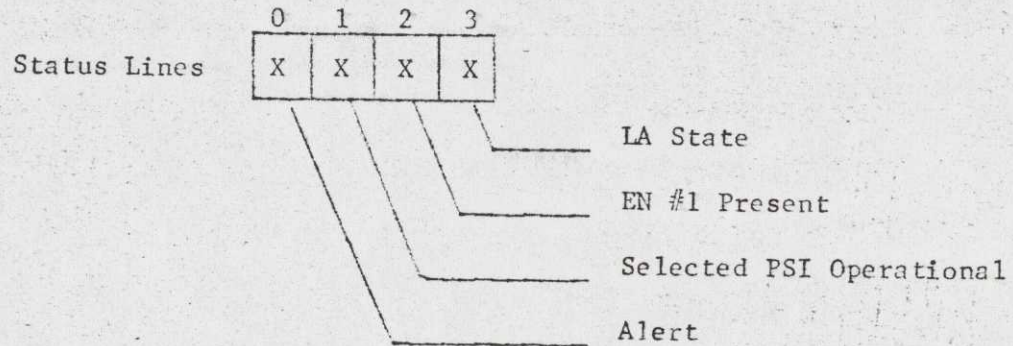
- L stands for "Load" and indicates that each flip-flop of the addressed register is to be set or reset depending upon the logical value "1" or "0" of the corresponding IAI Data Out line.
- R stands for "Reset" and indicates that each flip-flop of the addressed register can only be reset. A flip-flop reset is carried out when the corresponding IAI Data Out line indicates "0".
- C stands for "clear" and indicates that all flip-flops of the addressed register are to be reset where the Set LA microcommand occurs. The content of the IAI Data Out bus is meaningless.

Register Address	Bit Index							
AC ₅₋₇	0	1	2	3	4	5	6	7
000-L	PSI Switch	Write Read	Backward Forward	Allow Parity Errors				
001-R					Drop of OPO PSI #1	Drop of OPO PSI #2	End of Ser. Code Sequence	Terminate
010-L	PSI #1 Operat. In	PSI #1 Reserve In	PSI #1 Meter In		PSI #2 Operat. In	PSI #2 Reserve In	PSI #2 Meter In	
011-L*						Service Code In	Service Enable Out	Strobe In
100-C	Address Control Parity Error	PSI Buffer Parity Error	Upper IAI DO Lines Parity Error	Lower IAI DO Lines Parity Error				

* The register 011 is addressed by a Test LA microcommand for the purpose of diagnosis only.

4.4.1 (cont'd.)

When a Set LA microcommand occurs, the following status is sent along with "Response In" on the IAI Status lines to the MPC.



$STAT_0 = 1$ indicates that a parity error has been detected on the Address/Control lines or on the Data Out lines of the IAI during the current microcommand execution.

$STAT_1 = 1$ indicates that the operational out line of the selected PSI is up.

$STAT_2 = 1$ indicates that the LA requires a data transfer service.

$STAT_3 = 1$ indicates that the LA is in the "idle" state,

otherwise, $STAT_{0-3} = 0$

4.4.1.1 Set LA Mode

This Set LA submicrocommand defined by $AC_{4-7} = 0000$ is used to initialize the LA before a data transfer, or before a service code transfer if the two PSI switch is not properly selected.

The Set LA Mode submicrocommand sets the LA to a known state according to the parameters transmitted along with Address/Control on the Data Out bus of the IAI.

This submicrocommand resets all previous errors memorized within the LA.

Address/Control

0	1	2	3	4	5	6	7
1	0	0	X	0	0	0	0

LA State

$AC_3 = 0$ does not affect the LA state

$AC_3 = 1$ sets up the LA in the "busy" state

Data Out

0	1	2	3	4	5	6	7
X	X	X	X				

Meaningless

Allow Parity Error

Forward or Backward

Read or Write

Two PSI Switch Selection

The following parameters define the position of the switch and the LA mode for the subsequent data transfer.

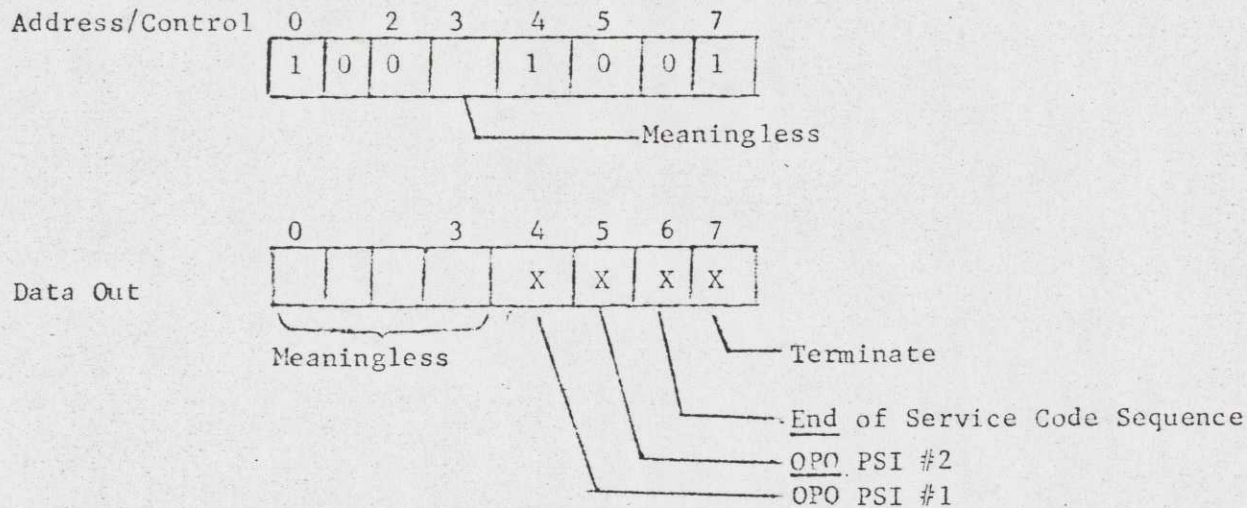
DO_0	= 0	PSI #1 selection
DO_0	= 1	PSI #2 selection
DO_1	= 0	Read Mode
DO_1	= 1	Write Mode
DO_2	= 0	Set Forward Mode
DO_2	= 1	Set Backward Mode
DO_3	= 0	Request the LA to transmit data with a correct parity
DO_3	= 1	Request the LA to transmit data as they were received

4.4.1.2 Reset Cause of an EN #2

This Set LA submicrocommand defined by $AC_{47} = 1001$ allows the following causes of an EN #2 to be reset.

- Drop of Operational Out on PSI #1 *
- Drop of Operational Out on PSI #2 *
- End of Service Code Sequence
- End of Data Transfer Sequence

* NOTE: The EN #2 register memorizes the falling edge of an Operational Out drop.

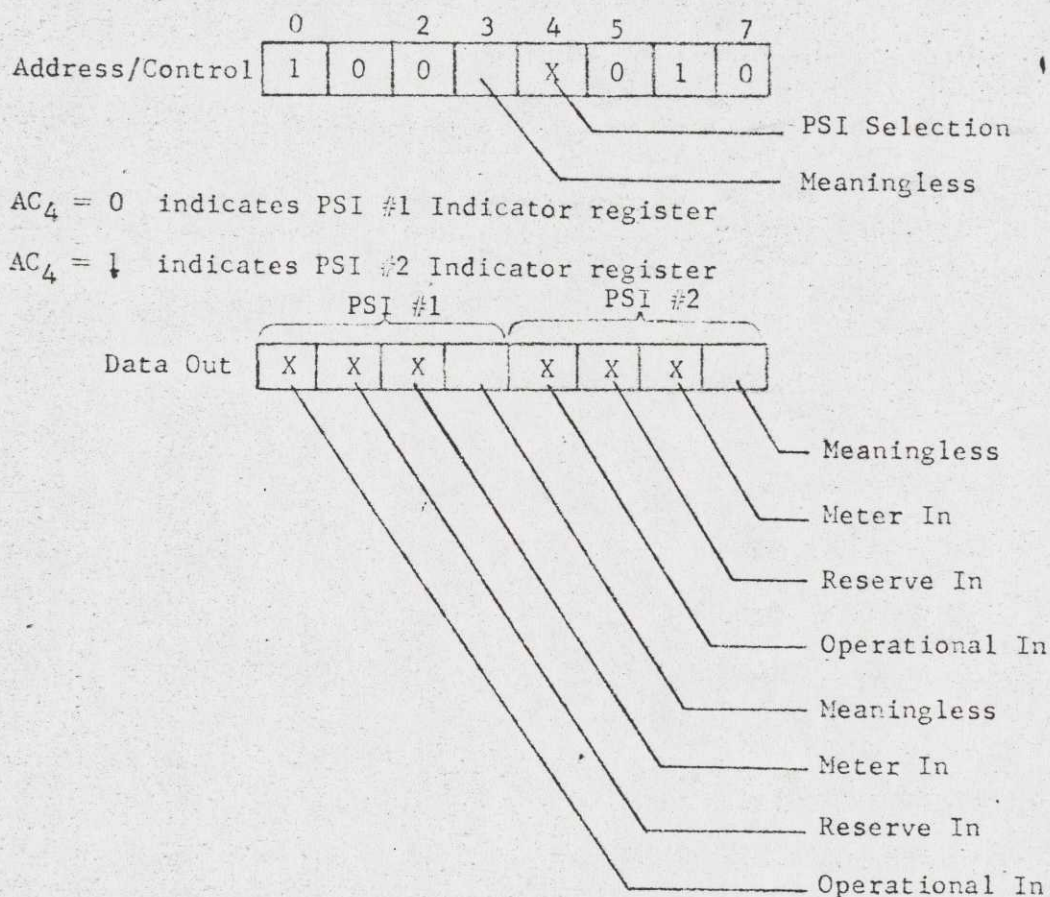


A "0" on one of the Data Out-Lines will reset the corresponding flip-flop.

If a Data Out-Line indicates 1, the corresponding flip-flop is not affected.

4.4.1.3 Set/Reset PSI Indicator Register

This Set LA Submicrocommand defined by $AC_{5-7} = 010$, provides the capability of loading the various flip-flops associated with the PSI #1 and PSI #2 indicator registers.



Each flip-flop of the Indicator Register is set or reset depending upon the value 1 or 0 of the corresponding Data Out line of the IAI.

4.4.1.4 Reset Errors

This Set LA submicrocommand defined by $AC_{5-7} = 100$ resets all errors memorized in the Link Adaptor

- IAI Address/Control lines parity error
- PSI Buffer parity error
- IAI Data Out Lines parity error

AC_{3-4} and the contents of the IAI Data Out Lines are meaningless.

4.4.2 Data Transfer Microcommand

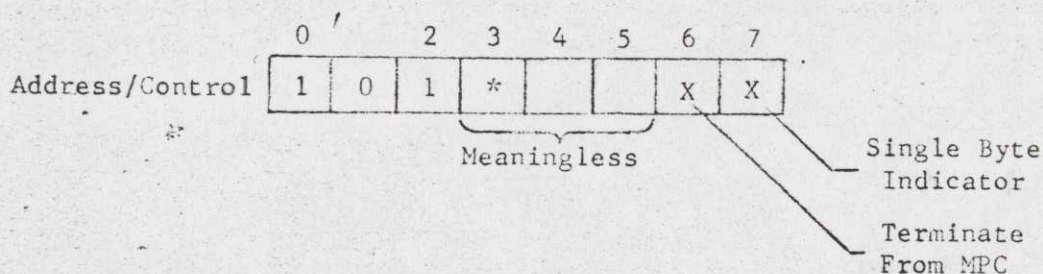
This microcommand defined by $AC_{0-2} = 101$ on the Address/Control lines of the IAI controls the transfer of data between the LA and the MPC according to the mode previously set in the LA

Read Mode: data is transferred from MPC to LA on the IAI Data Out bus.

Write Mode: data is transferred from LA to MPC on the IAI Data In bus.

Forward Mode: data is transferred left justified on the IAI data lines.

Backward Mode: data is transferred right justified on the IAI data lines.



$AC_6 = 1$ indicates that a data transfer termination is initiated by the MPC. The PSI signal "Terminate In" shall be generated by the LA to the external system with the last byte to be transferred, at the next opportunity.

$AC_7 = 1$ indicates a one byte transfer on the IAI data out bus. AC_7 is used in the Read mode to indicate whether one or two bytes of data are transferred from the MPC to the LA.

In the Forward mode, a one byte transfer is left justified on the IAI Data Out Lines.

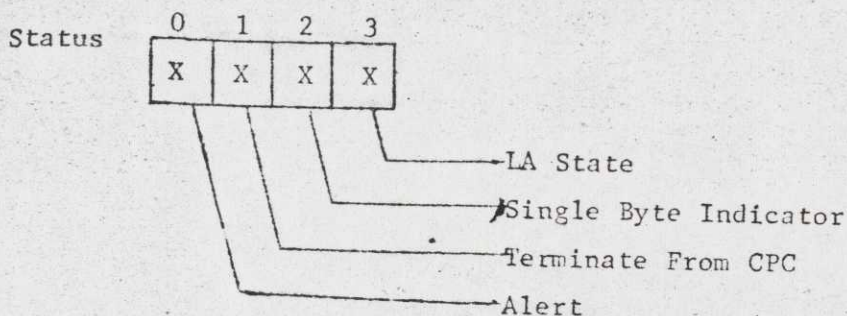
In the Backward Mode, a one byte transfer is right justified on the IAI Data Out Lines.

AC_7 must be 0 in the Write Mode

* AC_3 is reserved for CA use and is meaningless for the LA (See 4.5).

4.4.2 (Cont'd.)

When a Data Transfer microcommand occurs, the following status is sent along with "Response In" on the IAI status lines to the MPC:



$STAT_0 = 1$ indicates that at least one of the following errors has been detected by the LA during a previous Data transfer microcommand.

- IAI Address/Control lines parity error
- PSI buffer parity error
- IAI Data Out Lines parity error
- Selected PSI non-operational
- Data transfer microcommand activated during a Service Code Sequence.

$STAT_1 = 1$ indicates that a data transfer termination has been initiated by the Central Processor Complex.

$STAT_2 = 1$ indicates a one byte transfer on the IAI Data In bus.

$STAT_2$ is used in the Write mode to indicate whether one or two bytes of data are transferred from the LA to the MPC.

In the Forward Mode, a one byte transfer is left justified on the IAI Data In Lines.

In the Backward Mode, a one byte transfer is right justified on the IAI Data In Lines.

$STAT_2$ must be 0 in the Read Mode.

$STAT_3 = 1$ indicates that the LA is in the "idle" state.

Otherwise $STAT_{0-3} = 0$

4.4.2 (cont'd)

A Data Transfer microcommand is normally executed with the LA in the "busy" state. The microcommand is tied up until the LA is ready for a data service. The IAI Line "Response In" is used to indicate that data on the Data Out lines to the LA has been accepted, or that data is available on the Data In Lines from LA.

If the MPC initiates a Data transfer microcommand when the LA is "idle," the LA ignores the command and sends back "Response In" with the status "idle" on the status line STAT₃.

If the LA is "busy" but within a service code sequence, the LA ignores the command and sends back "Response In" with the status "alert" on the status line STAT₀.

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4.4.3 Service Code Transfer microcommand

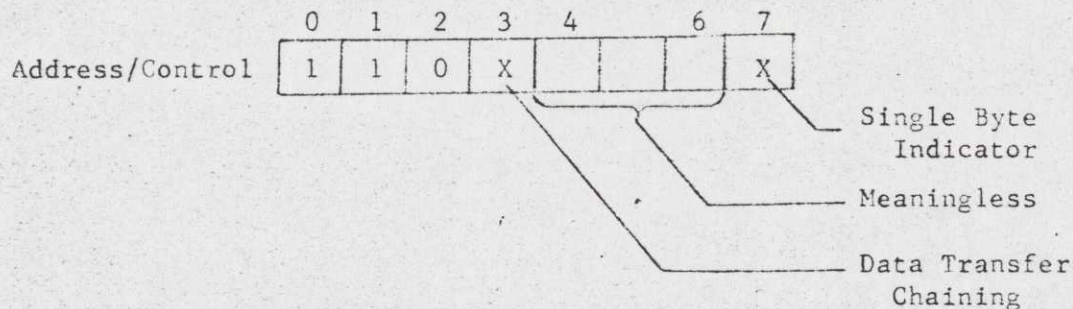
This microcommand, defined by $AC_{0-2} = 110$ on the Address/Control lines of the IAI controls the transfer of a Service Code to the external system attached to the Link Adapter. The Two-PSI switch must be properly selected.

The Service Code Transfer microcommand overrides the data transfer mode currently set in the LA for the duration of the service code sequence.

A service code transfer is always carried out in the adequate mode, independent of the mode currently set in the LA.

The Service Code to be transferred to the external system is transmitted along with Address/Control on the IAI Data Out bus.

The PSI signal "Service Code In" shall be generated to the external system by the LA.



$AC_3 = 1$ indicates that the current service code sequence is followed by a data transfer sequence, and that the LA must stay in the "busy" state to request data services from both the MPC and CPC.

$AC_7 = 1$ indicates to the LA that the Service Code to be transferred is made up of one byte, available on the lower lines of the IAI Data Out bus.

$AC_7 = 0$ indicates a two byte Service Code.

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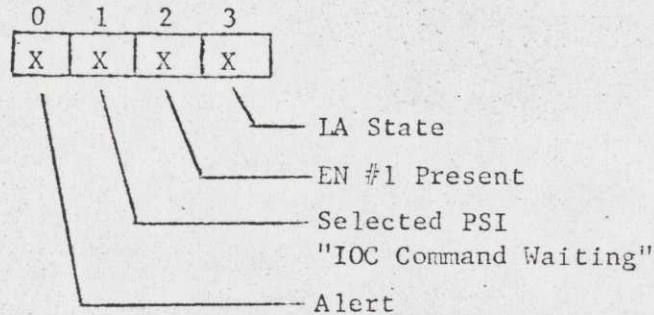
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4.4.3 (cont.)

When a Service Code Transfer microcommand occurs, the following status is sent along with "Response In" on the IAI Status lines to the MPC:

Status lines



STAT₀ = 1 indicates that at least one of the following errors has been detected by the LA during the current microcommand

- IAI Address/Control lines parity error
- IAI Data Out lines parity error
- Selected PSI non-operational
- Service Code Transfer microcommand activated while the LA is in the "busy" state.

STAT₁ = 1 indicates that the "IOC Command Waiting" line of the selected PSI is up.

STAT₂ = should be 0 for this microcommand. STAT₂ may reflect an EN #1 if the LA is abnormally "busy".

STAT₃ = indicates the LA state and should reflect that the LA is in the "idle" state (STAT₃ = 1).

A Service Code transfer microcommand is normally activated while the LA is in the "idle" state. If the selected PSI is non-operational, the command is ignored and "alert" is sent back on STAT₀ to the MPC.

If the MPC initiates a Service Code transfer microcommand when the LA is "busy", the LA ignores the command and sends back "Response In" with "alert" and "busy" on the status lines STAT₀ and STAT₃.

If the PSI line "IOC Instruction Waiting" is up at the end of a Service Code sequence, the LA comes back to the "idle" state, whether or not the Service Code transfer microcommand has requested the LA to stay in the "busy" state.

4.4.4

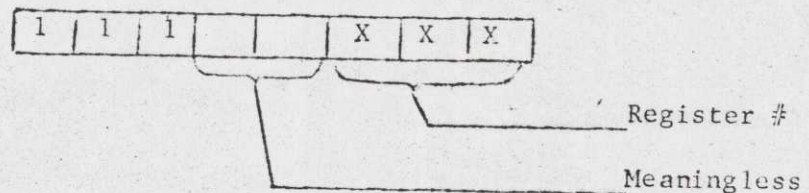
Test LA Microcommand

This microcommand, defined by AC₀₋₂=111 on the Address/Control lines of the IAI, is used to read:

- The mode of operation of the LA and the two PSI switch position
- The cause of an EN #2
- The status of some PSI lines
- Any error memorized within the LA
- The content of any control register for the purpose of diagnosis.

The Test LA microcommand provides the capability to read out on the 8 lower lines of the IAI Data In bus (DI₃₋₁₅) the contents of the LA register addressed by AC₅₋₇.

Address/Control



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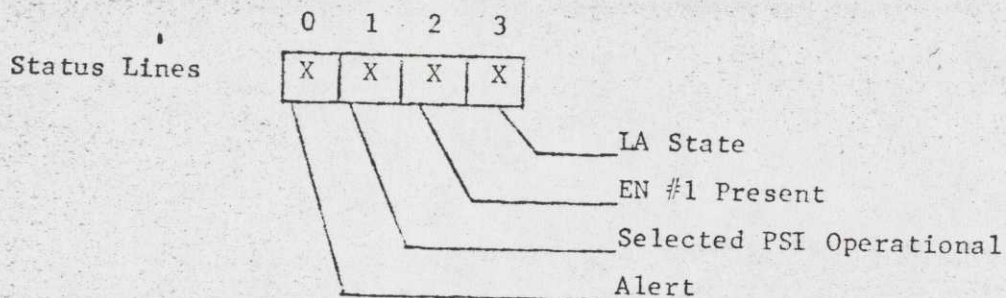
4.4.4 (cont.)

The following table shows the contents of the various IA registers which can be read out under microprogram control either for a normal use or for the purpose of diagnosis.

Register Address ACS-7	BIT INDEX							
	0	1	2	3	4	5	6	7
000	Two PSI Switch	Write Read	Backward Forward	Allow Parity Errors		PSI Buffer Full	A-IAI Buffer Full	B-IAI Buffer Full
001	PSI #1 CPW	PSI #2 CPW	PSI #1 IIW	PSI #2 IIW	PSI #1 Drop of OPO	PSI #2 Drop of OPO	End of Serv.Code Sequence	Termin-ate
010	PSI #1 Operat. In	PSI #1 Reserve In	PSI #1 Meter In	PSI #1 Meter Out	PSI #2 Operat. In	PSI #2 Reserve In	PSI #2 Meter In	PSI #2 Meter Out
011						Service Code In	Service Enable Out	Strobe In
100	Address Control Parity Error	PSI Buffer Parity Error	Upper IAI DO Lines Parity Error	Lower IAI DO Lines Par. Error			Selected PSI Operat. In	Selected PSI Operat. Out
101			PSI - - B U F F E R					
110			A - - IAI - - B U F F E R					
111			B - - IAI - - B U F F E R					

4.4.4 (Cont'd.)

When a test LA microcommand occurs, the following status is sent along with "Response In" on the IAI Status lines to the MPC.



STAT₀ = 1 indicates that a parity error has been detected on the Address/Control lines or on the Data Out lines of the IAI during the current microcommand execution.

STAT₁ = 1 indicates that the "Operational Out" line of the selected PSI is up.

STAT₂ = 1 indicates that the LA requires a data transfer service.

STAT₃ = 1 indicates that the LA is in the "idle" state

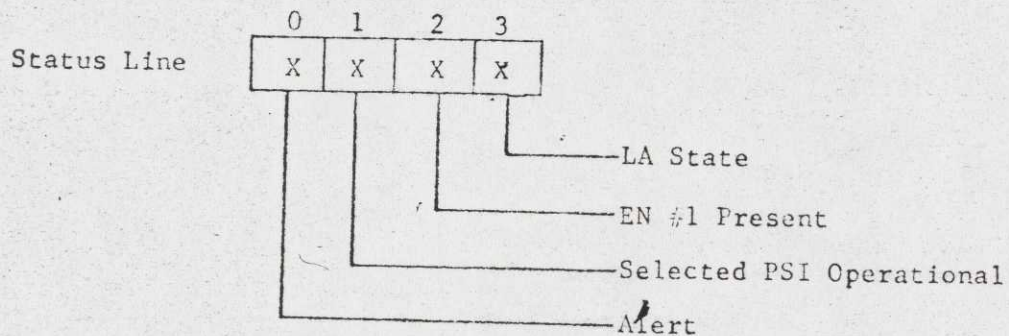
Otherwise, STAT 0-3 = 0.

4.4.5 Clear LA microcommand

This microcommand defined by $AC_0 = 0$ and $AC_{1-7} = 1$ on the Address/Control lines of the IAI resets all errors and abnormal conditions memorized in the LA and sets it up in a known state.

- PSI #1 selected
- Write mode
- Forward mode
- Idle state

The PSI indicator register is not affected by the Clear LA microcommand. Status reflected back to the MPC are the same as for a SET LA microcommand.

4.4.6 Adapter Identification microcommand

This microcommand, defined by $AC_{0-7} = 0$ on the Address/Control lines of the IAI is used to identify the adapter attached to each part of the MPC.

A code of all zeros on the IAI Data in lines is sent along with "Response In" whenever this microcommand is received by a PSI Link Adapter.

The Adapter Identification microcommand affects neither the LA state nor the LA mode but may affect the Error register if any error is detected during the execution of the microcommand.

Status reflected back to the MPC is the same as for a Set LA microcommand.

4.5 Link Adapter/Controller Adapter Interface

Four special lines which are not part of the standard internal Adapter Interface are available to or from the LA through the MPC backpanel.

These lines, which are not visible from the basic MPC, can be sampled independently of an LA or a CA selection. They are defined as follows:

- Alert: This line, from LA to DA's, reflects any errors memorized within the LA, or a non-operational selected PSI channel.
- LA Available: This line from LA to DA's indicates that a Data transfer microcommand is not going to be tied up by RPI.

This line is up when the LA is either in the "idle" state or in the "busy" state but ready for a data service.

- Hold RPI: This line from CA to LA is used to hold the generation of the IAI signal "Response In" to the MPC when an LA microcommand is to be carried out.

When the CA enables "Response In" the microcommand shall be normally executed by the LA.

Two "Hold RPI" lines are available, one from CA₀ and one from CA₁.

Note: The MPC has provision to execute two concurrent data transfer through the "Data In" and "Data Out" lines of the IAI under the control of a single DAI microinstruction. This feature allows a Data Transfer microcommand addressed to the LA to control a simultaneous data transfer with the associated CA.

The bit AC₃ of the IAI Address/Control bus indicates to the CA whether or not data are to be transferred between the CA and the MPC. This bit is meaningless for the LA.

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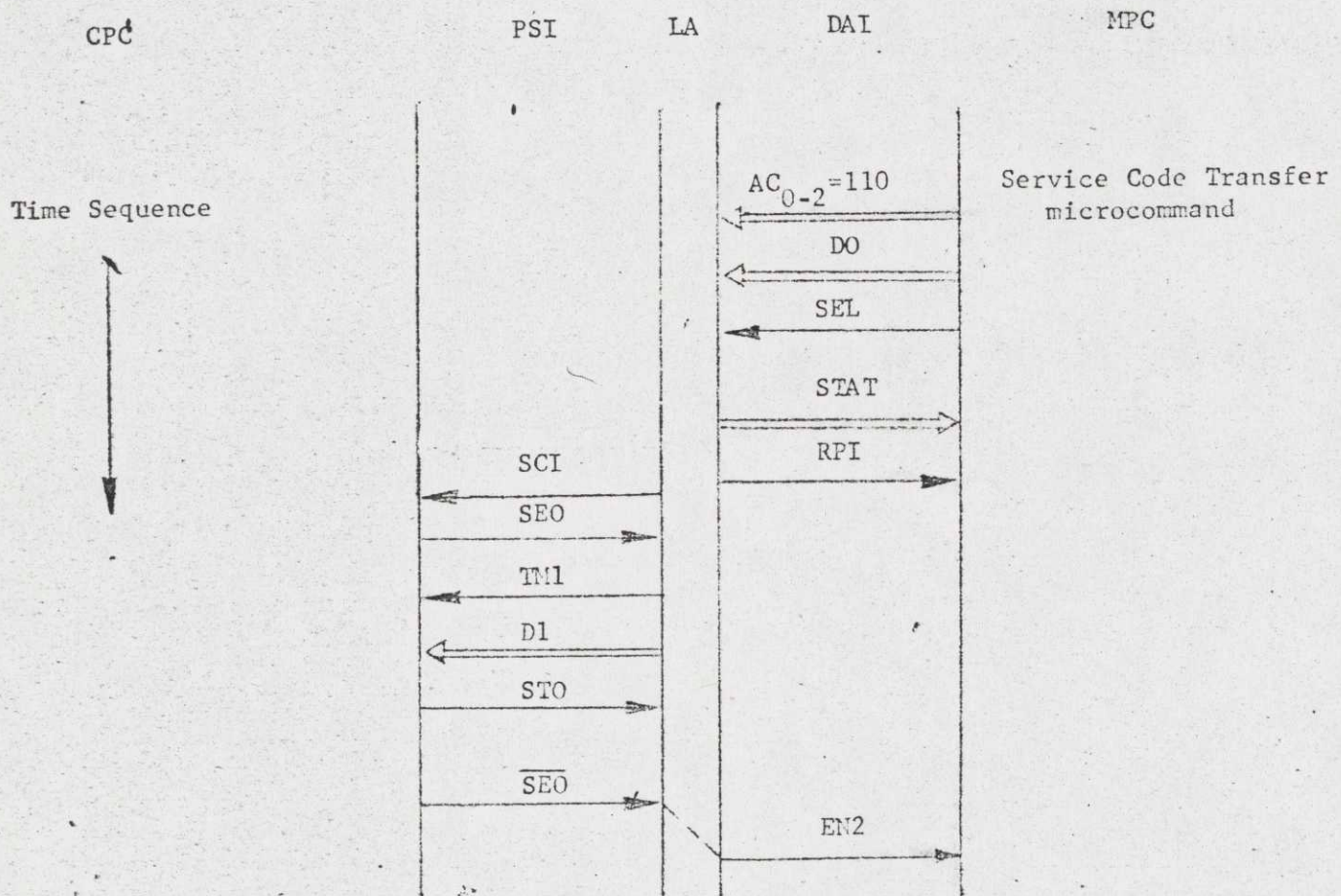
4.6

Basic Dialog Sequences

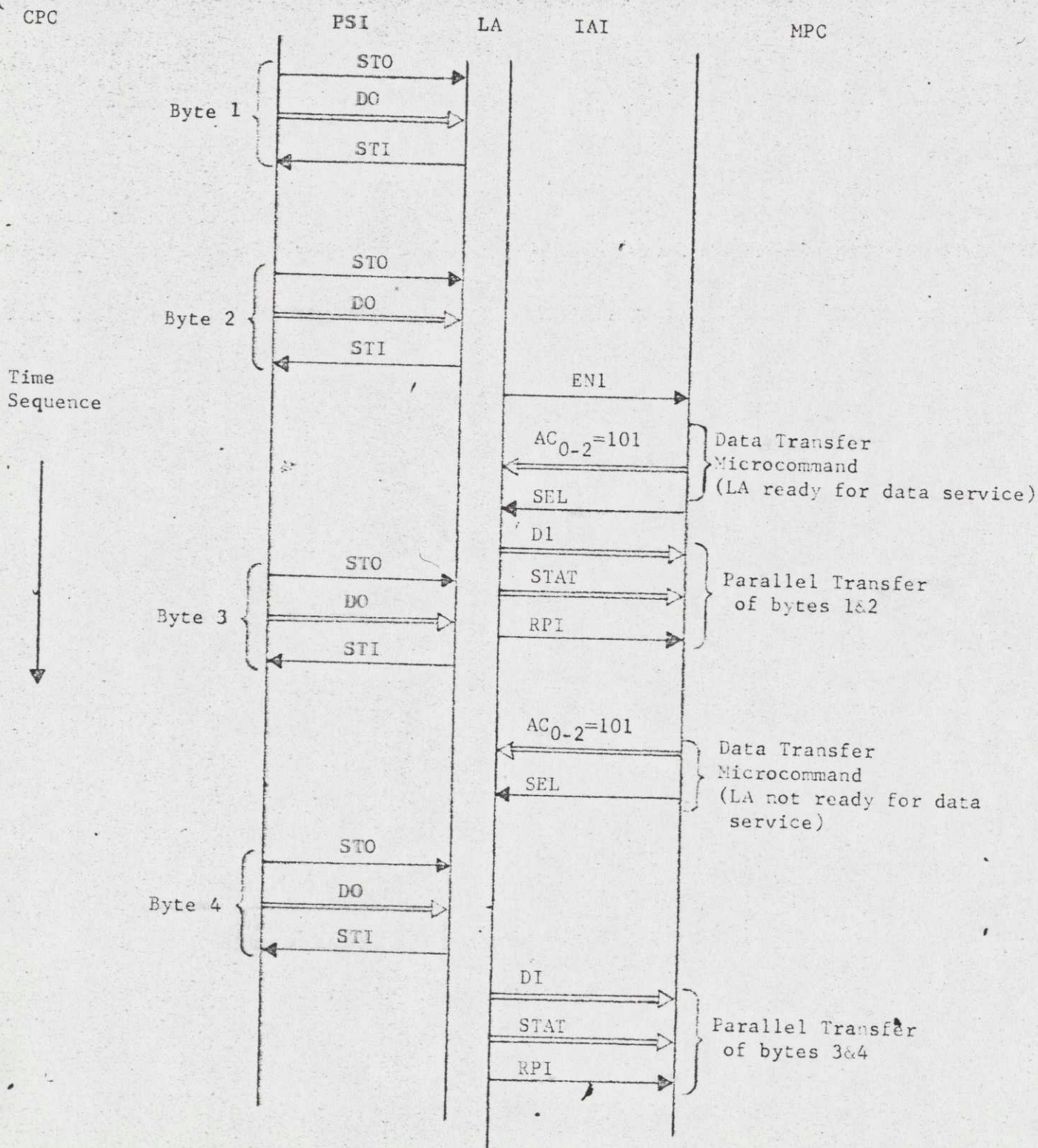
The overall dialog on the Processor Subsystem Interface can be handled by using three basic dialog sequences:

- Service code transfer
- Data Transfer in Write mode
- Data Transfer in Read mode

The following charts show the relative sequence of signals exchanged on the PSI and the LAI for each sequence.

4.6.1 Service Code Transfer (assuming a one byte Service code)

4.6.2 Data Transfer in Write Mode (The LA buffers are assumed empty at the beginning of the sequence)



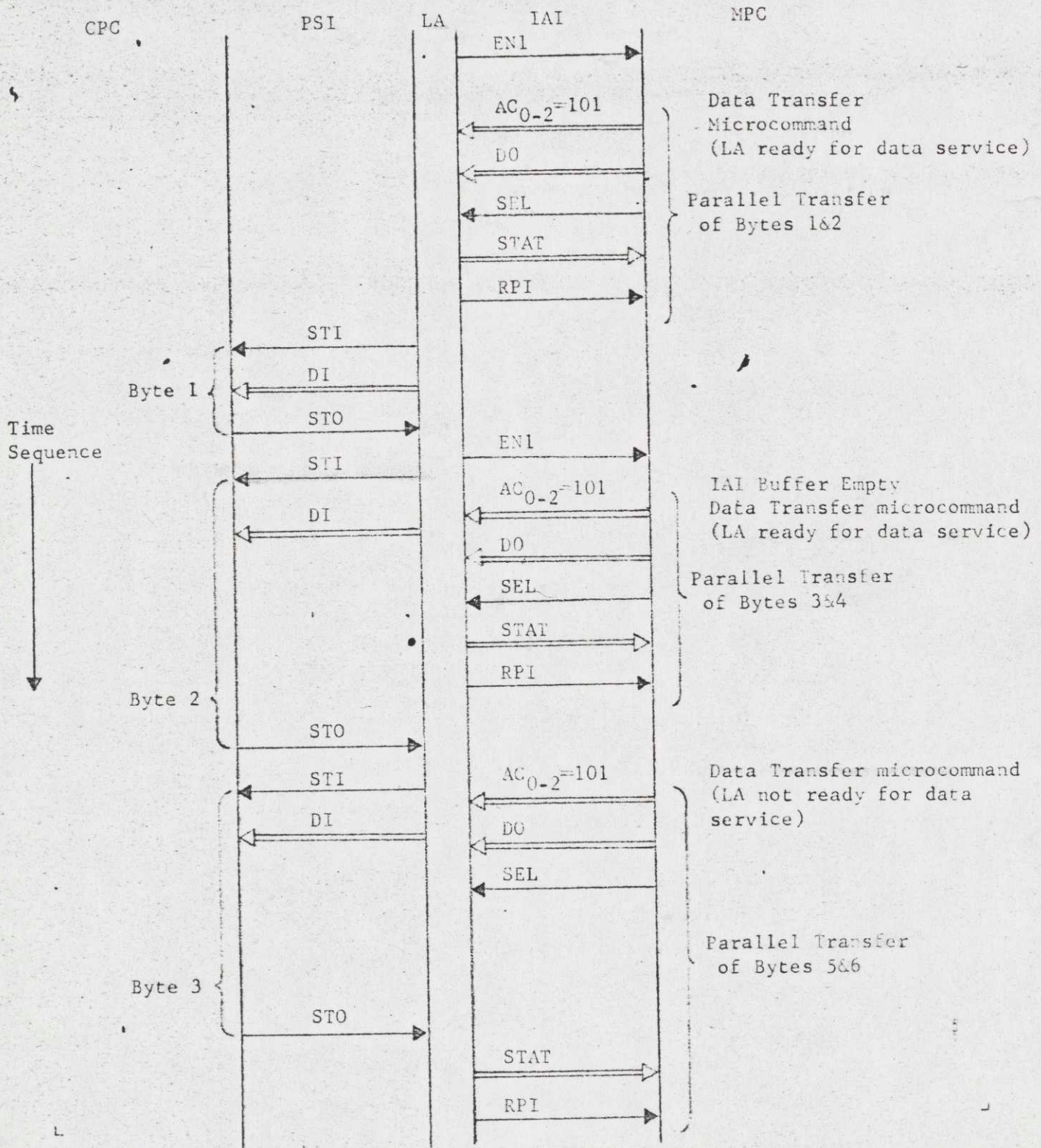
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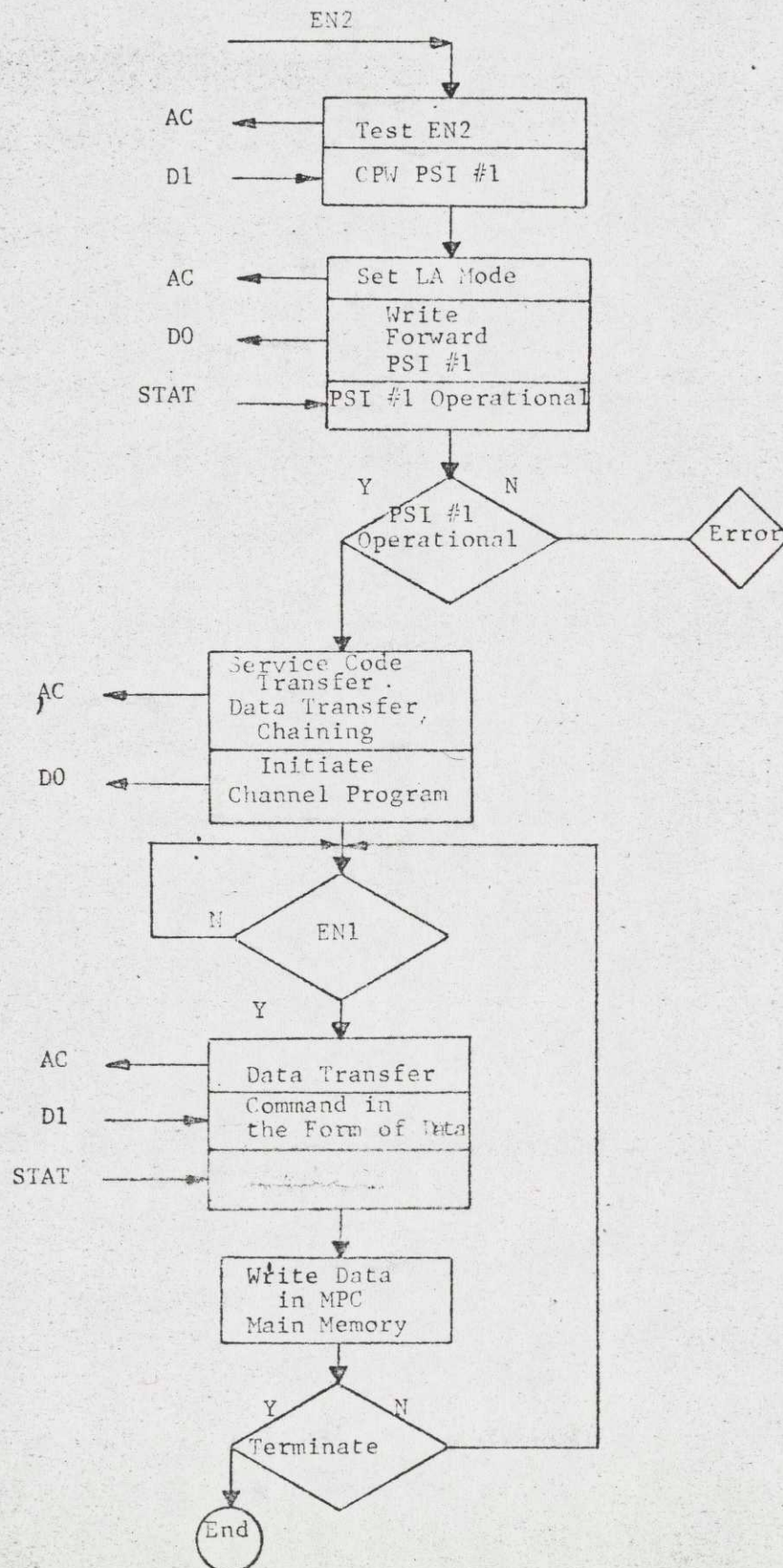
4.6.3

Data Transfer in Read Write (The LA buffers are assumed empty at the beginning of the sequence)



4.7

Example of Operation: Command Transfer



5.0 GENERAL DECISION REQUIREMENTS

The PSI-LA shall conform to the general design requirements contained in the GE-655 General Design Requirements EPS-1, 43A177851.

5.1 Physical Packaging

The Link Adapter will be packaged in the same cabinet as the MPC, using the same circuit set and packaging techniques.

5.2 Connectability

The MPC provides interfaces for two Link Adapters on Device Adapter ports 2 and 3.

5.3 Power Supply

The Link Adapter will use the same Power supply as the MPC.

5.4 Clock & Timing Requirements

The Link Adapter will use the same clock as the MPC:

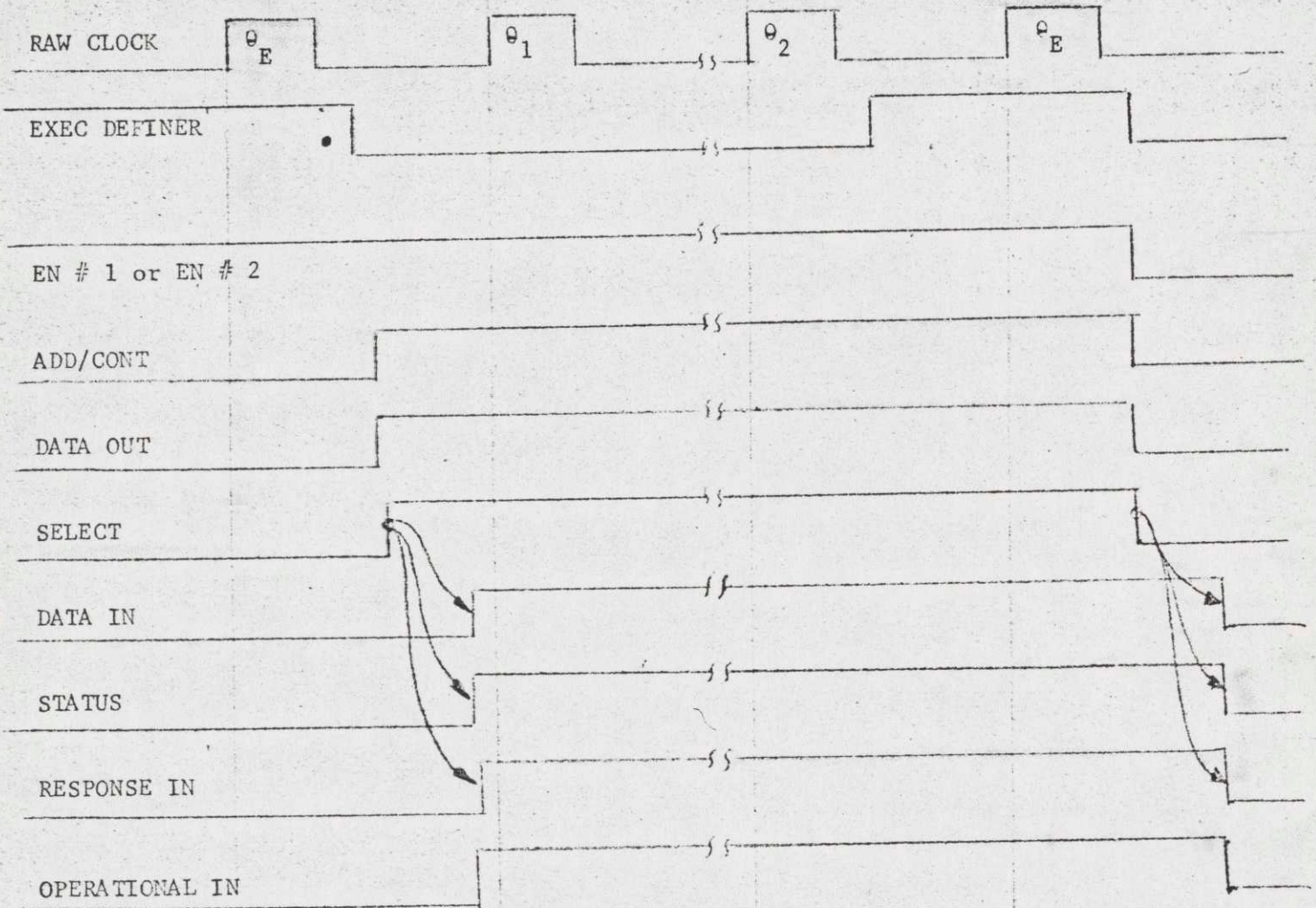
θ Execution, θ_1 , θ_2

The following diagram shows the timing relationships for the MPC-LA Interface.

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NOTE: The IA design should take into consideration the effects of signal transition times on the PSI. Although transition time should not generally be a problem, some cases may exist due to variation in circuit tolerance or short cable length, where transition time must be considered. The general design rule is that the Link Adapter must fully recognize the transition of a signal from one state to the other before any result of the transition can be returned to the external system.

6.0

RELIABILITY & MAINTAINABILITY REQUIREMENTS

The Link Adapter shall be designed to meet the Maintainability performance requirements defined in the common MPC Maintainability Specification 43A237500.

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